Amendments to the Claims:

Please cancel claims 4-7, 10-13 and 16-20, amend claims 1, 2, 8-9 and 14 and add new claims 21-29.

This listing of claims will replace all prior versions and listings of claims in the application.

1. (previously presented) A method for refreshing data in a dynamic circuit element having an input terminal and an output terminal, the method comprising:

(a) coupling ~~a static loop to the dynamic circuit element as~~ a feedback path from the output terminal to the input terminal to create a static loop;

(b) clocking the dynamic circuit element with complementary clock signals;

~~(b)~~(c) providing a separate control signal to the static loop;

~~(c)~~(d) ~~activateing~~ activating the static loop via the control signal to refresh the data in the dynamic circuit element.

2. (previously presented) The method of claim 1 further comprising ~~the operation of~~:

setting the control signal equal to approximately zero to deactivate the static loop so that the dynamic circuit element operates in a dynamic mode.

3. (currently amended) The method of claim 1 wherein the dynamic circuit element is an inverter included in a dynamic register.

4-7. (canceled)

8. (previously presented) A method for refreshing a dynamic register, the dynamic register comprising a first transmission gate and a second transmission gate operating in accordance with complementary clock signals, a first inverter disposed between the first and second transmission gates, a second inverter disposed at the output of the second transmission gate, the first inverter

having a first input terminal and a first output terminal, the second inverter having a second input terminal and a second output terminal, the method comprising the operations of:

(a) coupling ~~a first static loop to the first inverter as~~ a feedback path from the first output terminal to the first input terminal to create a first static loop;

(b) coupling ~~a second static loop to the second inverter~~ a feedback path from the second output terminal to the second input terminal to create a second static loop;

(c) providing a control signal separate from the complementary clock signal to the first and second static loops; and

(d) ~~activateing~~ activating the first and second static loops via the control signal to refresh the dynamic register.

9. (previously presented) The method of claim 8 further comprising ~~the operation of~~:

setting the control signal equal to approximately zero to deactivate the first and second static loops so that the dynamic register operates in a dynamic mode.

10-13. (canceled)

14. (previously presented) A system for refreshing a dynamic register, the dynamic register comprising a first transmission gate and a second transmission gate operating in accordance with complementary clock signals, a first inverter disposed between the first and second transmission gates, a second inverter disposed at the output of the second transmission gate, the first inverter having a first input terminal and a first output terminal, the second inverter having a second input terminal and a second output terminal, the system comprising:

(a) a first static loop coupled to the first inverter as a feedback path from the first output terminal to the first input terminal, the first static loop ~~directly~~ receiving a control signal ~~that is separate from the complementary clock signals~~, the first static loop being activated or deactivated by the control signal, the first static loop refreshing the first inverter when activated; and

(b) a second static loop coupled to the second inverter as a feedback path from the second output terminal to the second input terminal, the second static loop ~~directly~~ receiving a control signal ~~that is separate from the complementary clock signals~~, the second static loop being activated or deactivated by the control signal, the second static loop refreshing the second inverter when activated.

15. (original) The system of claim 14 wherein the first and second static loops are deactivated when the control signal is approximately equal to zero.

16-20. (canceled)

21. (new) A method for refreshing data in a system having a dynamic circuit element, the dynamic circuit element having an input terminal and an output terminal, and a static loop that forms feedback path from the output terminal to the input terminal, the method comprising:

(a) clocking the dynamic circuit element using clocking signals; and

(b) refreshing the dynamic circuit element via the static loop using a control signal.

22. (new) The method of claim 21 wherein the dynamic circuit element comprises an inverter.

23. (new) The method of claim 21 wherein refreshing the dynamic circuit element comprises activating the static loop via the control signal.

24. (new) The method of claim 23 further comprising:

setting the control signal equal to approximately zero to deactivate the static loop.

25. (new) The method of claim 21 further comprising coupling the static loop to the dynamic circuit element.

26. (new) A data system comprising:

a dynamic circuit element having an input terminal and an output terminal, and that operates in accordance with clocking signals; and

a static loop that forms a feedback path from the output terminal to the input terminal and refreshes the dynamic circuit element in accordance with a control signal.

27. (new) The data system of claim 26 wherein the dynamic circuit element comprises an inverter.

28. (new) The data system of claim 26 wherein the control signal activates or deactivates the static loop.

29. (new) The data system of claim 28 wherein the static loop refreshes the dynamic circuit when the static loop is activated.